Iterative Design of the Miller Operational Amplifier

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Abstract

An iterative approach to the design of the Miller Operational Amplifier (OA) is presented. Its main advantage over the many design procedures reported in the literature is the wider set of specifications it considers, particularly the power consumption. As example, the design of OA in a standard 150nm CMOS process using Cadence ADE GXL is presented. Simulation results validate the design, which meets the specifications: GBW of 100MHz, 500MHz and 1GHz for IDD=500uA AO=60dB PM=60dgr for CL=1pF.